1. A data transfer interface, comprising:

a first receiver and driver pair coupled to a first segment of a first data bus, said first receiver and driver pair being configured to receive data on said first segment using said first receiver and selectively place data on said first segment using said first driver;

a second receiver and driver pair coupled to a second segment of said first data bus, said second receiver and driver pair being configured to receive data on said second segment using said second receiver and selectively place data on said second segment using said second driver; and

an selector circuit connected to said first and second receiver and driver pairs, said selector circuit selectively operating said first and second receiver and driver pairs according to a selection signal such that in a first operating mode said first receiver and driver pair passes data between said first bus segment and an I/O device, and in a second operating mode said first and second receiver and driver pairs pass data between respective adjacent bus segments and bypass said I/O device.

2. An interface as in claim 1, wherein said selection signal operates to select said selector circuit and when said selection signal selects said selector circuit, said first and second receiver and driver pairs operate in said first operating mode.

3. An interface as in claim 1, wherein said selection signal operates to select said selector circuit and when said selection signal does not select said selector circuit, said first and second receiver and driver pairs operate in said second operating mode.

4. An interface as in claim 1, wherein said selection signal operates to select said selector circuit and when said selection signal selects said selector circuit, said second receiver and driver pair is deactivated to permit point-to-point data communications using said first receiver and driver pair between said I/O device and another device connected to said first data bus.

5. An interface as in claim 1, wherein said first and second receiver and driver pairs are located on a same integrated circuit as a memory device.

6. An interface as in claim 1, wherein said first and second receiver and driver pairs are located on a memory module.

7. An interface as in claim 1, wherein said I/O device comprises a memory device.

8. An interface as in claim 1, wherein said I/O device comprises a second data bus.

9. A data transfer interface, comprising:

a first receiver and driver pair coupled to a first segment of a first data bus, said first receiver and driver pair being connected to receive data on said first segment using said first receiver and selectively place data on said first segment using said first driver;

a second receiver and driver pair coupled to a second segment of said first data bus, said second receiver and driver pair being connected to receive data on said second segment using said second receiver and selectively place data on said second segment using said second driver; and

an interface circuit coupled to said first and second receiver and driver pairs and a second data bus, wherein said interface circuit is configured to receive data from said first receiver and selectively place said data on said second data bus, and receive data on said second data bus and selectively place said data on said first data bus.

10. The interface of claim 9, wherein said interface circuit selects data for receipt from said first and second data buses according to a selection signal received on a command and address bus.

11. The interface of claim 9, wherein said interface circuit is further configured to receive a selection signal, and said interface circuit selectively deactivates said second receiver and driver pair according to said selection signal.

12. The interface of claim 11, wherein said interface circuit deactivates said second receiver and driver pair when said selection signal instructs said interface circuit to transfer data between said first and second data buses.

13. The interface of claim 11, wherein said interface circuit is connected in a point-to-point data connection with another device connected to said first data bus when said second receiver and driver pair is deactivated.

14. The interface of claim 11, wherein said selection signal is received on a command and address bus.

15. The interface of claim 9, wherein said first receiver and driver pair is coupled to said first segment via a first set of I/O pins, and said second receiver and driver pair is coupled to said second segment via a second set of I/O pins.

16. The interface of claim 9, wherein said interface circuit further comprises at least one of a multiplexer and demultiplexer that performs a data rate conversion between said first and second data buses.

17. The interface of claim 9, wherein said interface circuit further comprises a multiplexer and a demultiplexer which perform data rate conversions for data received on said first data bus that is placed on said second data bus and for data received on said second data bus that is placed on said first data bus.

18. The interface of claim 9, wherein said interface circuit further comprises at least one of a coder and decoder that performs at least one of a data encoding and decoding conversion between said first and second data buses.

19. The interface of claim 9, wherein said interface circuit further comprises a voltage converter that performs a voltage level conversion between said first and second data buses.

20. The interface of claim 9, wherein said first bus includes a first number of data paths and said second bus includes a second number of data paths, and said first number of data paths is less than said second number of data paths.

21. The interface of claim 9, wherein said second data bus is connected to at least one memory device.

22. The interface of claim 9, wherein said first data bus is connected to a memory controller.

23. The interface of claim 9, wherein said first data bus is connected to a processor.

24. The interface of claim 9, wherein said first data bus operates at a first data rate faster than a second data rate at which said second data bus operates.

25. The interface of claim 9, wherein said first data bus operates at a first voltage level less than a second voltage level at which said second data bus operates.

26. The interface of claim 9, wherein said first data bus transmits analog signals.

27. The interface of claim 9, wherein said first data bus transmits digital signals.

28. The interface of claim 9, wherein said first data bus transmits radio-frequency (RF) signals.

29. The interface of claim 9, wherein said first data bus is a multidrop bus.

30. The interface of claim 9, wherein said first data bus is a substantially stubless data bus.

31. A memory module, comprising:

at least one memory device;

a data transfer interface connected to a first data bus and to said at least one memory device by a second data bus, said data transfer interface comprising:

a first receiver and driver pair coupled to a first segment of a first data bus, said first receiver and driver pair being connected to receive data on said first segment using said first receiver and selectively place data on said first segment using said first driver;

a second receiver and driver pair coupled to a second segment of said first data bus, said second receiver and driver pair being connected to receive data on said second segment using said second receiver and selectively place data on said second segment using said second driver; and

an interface circuit coupled to said first and second receiver and driver pairs and a second data bus, wherein said interface circuit is configured to receive data from said first receiver and selectively place said data on said second data bus, and receive data on said second data bus and selectively place said data on said first data bus.

32. The memory module of claim 31, wherein said interface circuit selects data for transfer between said first and second data buses according to a selection signal received on a command and address bus.

33. The memory module of claim 31, wherein said interface circuit is further configured to receive a selection signal, and said interface circuit selectively deactivates said second receiver and driver pair according to said selection signal.

34. The memory module of claim 33, wherein said interface circuit deactivates said second receiver and driver pair when said selection signal instructs said interface circuit to transfer data between said first and second data buses.

35. The memory module of claim 33, wherein said interface circuit is connected in a point-to-point data connection with another device connected to said first data bus when said second receiver and driver pair is deactivated.

36. The memory module of claim 33, wherein said selection signal is received on a command and address bus.

37. The memory module of claim 31, wherein said first receiver and driver pair is coupled to said first segment via a first set of I/O pins, and said second receiver and driver pair is coupled to said second segment via a second set of I/O pins.

38. The memory module of claim 31, wherein said interface circuit further comprises at least one of a multiplexer and demultiplexer that performs a data rate conversion between said first and second data buses.

39. The memory module of claim 31, wherein said interface circuit further comprises a multiplexer and a demultiplexer which perform data rate conversions for data received on said first data bus that is placed on said second data bus and for data received on said second data bus that is placed on said first data bus.

40. The memory module of claim 31, wherein said interface circuit further comprises at least one of a coder and decoder that performs at least one of a data encoding and decoding conversion between said first and second data buses.

41. The memory module of claim 31, wherein said interface circuit further comprises a voltage converter that performs a voltage level conversion between said first and second data buses.

42. The memory module of claim 31, wherein said first bus includes a first number of data paths and said second bus includes a second number of data paths, and said first number of data paths is less than said second number of data paths.

43. The memory module of claim 31, wherein said second data bus is connected to at least one memory device.

44. The memory module of claim 31, wherein said first data bus is connected to a memory controller.

45. The memory module of claim 31, wherein said first data bus is connected to a processor.

46. The memory module of claim 31, wherein said first data bus operates at a first data rate faster than a second data rate at which said second data bus operates.

47. The memory module of claim 31, wherein said first data bus operates at a first voltage level less than a second voltage level at which said second data bus operates.

48. The memory module of claim 31, wherein said first data bus transmits analog signals.

49. The memory module of claim 31, wherein said first data bus transmits digital signals.

50. The memory module of claim 31, wherein said first data bus transmits radio-frequency (RF) signals.

51. The memory module of claim 31, wherein said first data bus is a multidrop bus.

52. The memory module of claim 31, wherein said first data bus is a substantially stubless data bus.

53. A data exchange system, comprising:

a first data bus having at least first and second bus segments;

a controller connected to place data on and receive data from said first data bus;

a processor coupled to said controller, and

a data transfer interface, comprising:

a first receiver and driver pair coupled to a first segment of a first data bus, said first receiver and driver pair being connected to receive data on said first segment using said first receiver and selectively place data on said first segment using said first driver;

a second receiver and driver pair coupled to a second segment of said first data bus, said second receiver and driver pair being connected to receive data on said second segment using said second receiver and selectively place data on said second segment using said second driver; and

an interface circuit coupled to said first and second receiver and driver pairs and a second data bus, wherein said interface circuit is configured to receive data on said first data bus and selectively place said data on said second data bus, and receive data on said second data bus and selectively place said data on said first data bus.

54. A data transmission system comprising:

a processor;

a least one memory subsystem connected to said processor; and

a bus coupled to each of a controller and at least one memory subsystem interface circuit of said at least one memory subsystem, whereby said memory subsystem interface circuit couples at least one memory device to said bus, said memory subsystem interface circuit comprising a circuit for receiving data from said bus and converting it to data which can be processed by said at least one memory device and for receiving data from said at least one memory device and converting it to data which can be transmitted over said bus;

wherein said at least one memory subsystem interface circuit includes first and second receiver and driver pairs connected to respective first and second segments of said bus, said first receiver and driver pair receiving data on said first segment using said first receiver and selectively placing data on said first segment using said first driver, and said second receiver and driver pair receiving data on said second segment using said second receiver and selectively placing data on said second segment using said second driver.

55. A system as in claim 54, wherein said controller resides on a same printed circuit board as said processor.

56. A system as in claim 54, wherein said controller is integrated into said processor.

57. A method of data communication between devices in an electronic circuit, comprising:

receiving data at first and second receivers coupled to respective first and second segments of a first data bus;

driving data using first and second drivers coupled to said respective first and second segments, said driving being performed according to a selection signal, such that in a first operating mode a first receiver and driver pair passes signals between said first segment of said first data bus and an I/O device, and in a second operating mode said first and a second receiver and driver pairs pass signals between respective adjacent bus segments and bypass said I/O device.

58. A method as in claim 57, wherein said I/O device comprises a memory device.

59. A method as in claim 57, wherein said I/O device comprises a second data bus.

60. A method of data communication between devices in an electronic circuit, comprising:

connecting an interface circuit having first and second receiver and driver pairs to respective first and second segments of a first data bus that operates at a first data rate;

connecting said interface circuit to a second data bus that operates at a second data rate;

receiving and transmitting data on said first data bus using said first and second receiver and driver pairs;

receiving and transmitting data on said second data bus;

selectively placing data received from said first bus segment on said second bus segment;

selectively placing data received from said second bus segment on said first bus segment; and

selectively converting data received from one of said first and second data buses for use on the other of said first and second data buses.

61. A method as in claim 60, wherein said selective conversion of data is performed according to a selection signal.

62. A method as in claim 61, wherein said selective conversion of data is performed when said interface circuit is selected for operation by said selection signal.

63. A method as in claim 61, wherein said selective conversion of data is not performed when said interface circuit is not selected for operation by said selection signal.

64. A method as in claim 61, wherein said second receiver and driver pair is deactivated when said interface circuit is selected for operation by said selection signal.

65. A method as in claim 61, wherein when said interface circuit is not selected for operation by said selection signal, data on said first segment of said first data bus is passed through to said second segment of said first data bus and data on said second segment is passed through to said first segment.

66. A method as in claim 60, wherein said first data rate is faster than said second data rate.

67. A method as in claim 60, further comprising converting received data between said first data rate of said first data bus and said second data rate of said second data bus.

68. A method as in claim 60, further comprising converting received data between a first encoding of said first data bus and a second encoding of said second data bus.

69. A method as in claim 60, further comprising converting received data between a first voltage level of said first data bus to a second voltage level of said second data bus.

70. A method as in claim 69, wherein said first voltage level is less than said second voltage level.

71. A method as in claim 60, wherein said first data bus connects to said first and second receiver and driver pairs using a first bus width different from a second bus width used to connect to said second data bus.

72. A method as in claim 71, wherein said first bus width is less than said second bus width.

73. A method as in claim 60, wherein devices of a first technology communicate with said interface circuit using said first data bus and devices of a second technology communicate with said interface circuit using said second data bus.

74. A method as in claim 73, wherein said devices of said first technology include at least one processor.

75. A method as in claim 73, wherein said devices of said second technology include at least one memory device.

76. A method as in claim 60, wherein said first data bus is a multi-drop bus.

77. A method as in claim 60, wherein said first data bus is a substantially stubless data bus.